WHAT IS CLAIMED IS:

1. A method for recycling a charge in a memory device, comprising:

performing a first refresh operation involving a first array of bit line sense amplifiers;

transferring charge from power lines of the first array of bit line sense amplifiers to power lines of a second array of bit line sense amplifiers involved in a second refresh operation performed subsequent to the first refresh operation; and

transferring charge from power lines of the first array of bit line sense amplifiers to power lines of a third array of bit line sense amplifiers involved in a third refresh operation performed subsequent to the second refresh operation.

2. The method of claim 1, further comprising transferring charge from power lines of the second array of bit line sense amplifiers to power lines of the third array of bit line sense amplifiers involved in the third refresh operation performed subsequent to the second refresh operation.

3. The method of claim 1, further comprising transferring charge from power lines of the first array of bit line sense amplifiers to power lines of at least a fourth array of bit line sense amplifiers involved in at least a fourth refresh operation performed subsequent to the third refresh operation.

4. The method of claim 3 further comprising transferring charge from power lines of the second and third arrays of bit line sense amplifiers to power lines of at least a fourth array of bit line sense amplifiers involved in at least a fourth refresh operation performed subsequent to the third refresh operation.

5. The method of claim 1, wherein transferring charge from power lines of the first array of bit line sense amplifiers to power lines of the second array of bit line sense amplifiers comprises:

closing one or more switches coupling the power lines of the first array of bit line sense amplifiers to one or more common recycle power lines; and

closing one or more switches coupling the power lines of the first array of bit line sense amplifiers to the one or more common recycle power lines.

6. The method of claim 1, further comprising performing at least one intermediate refresh operation between the first and second refresh operations, wherein charge is not transferred from power lines of the first array of bit line sense amplifiers to power lines of an array of bit line sense amplifiers involved in the intermediate refresh operation.

7. The method of claim 6, wherein after the third refresh operation, the voltage difference between the power lines of the first array of bit line sense amplifiers and a precharge level is approximately 25% of the voltage difference between the precharge level and the voltage level of the power lines immediately after the first refresh operation.

8. A method of recycling charge for use in a refresh operation involving an i^{th} array of bit line sense amplifiers of a memory device, where i is an integer, comprising:

precharging power lines of the i^{th} array of bit line sense amplifiers;

sequentially transferring charge from one or more power lines of N arrays of bit line sense amplifiers involved in previous refresh operations to one or more power lines of the i^{th} array, wherein N is an integer greater than 1 and the N arrays range from an $(i-N)^{th}$ array to an $(i-1)^{th}$ array; and

subsequently coupling the one or more power lines of the i^{th} array to one or more voltage supply lines.

9. The method of claim 8, wherein N is greater than 2.

10. The method of claim 8, wherein sequentially transferring charge from one or more power lines of the N arrays of bit line sense amplifiers to the one or more power lines of the i^{th} array comprises:

closing a first one or more switches to couple the one or more power lines of the i^{th} array to one or more common recycle lines; and

while the first one or more switches are closed, sequentially closing a plurality of sets of one or more switches, wherein closing each set couples one or more power lines of a different one of the N arrays of bit line sense amplifiers to the one or more common recycle lines.

11. A method for recycling a charge in a dynamic random access memory (DRAM) device, comprising:

performing a first refresh operation involving a first array of bit line sense amplifiers;

momentarily closing one or more switches to couple one or more power lines of the first array of bit line sense amplifiers to power lines of a second array of bit line sense amplifiers involved in a second refresh operation performed subsequent to the first refresh operation; and

momentarily closing one or more switches to couple one or more power lines of the first array of bit line sense amplifiers to power lines of a third array of bit line sense amplifiers involved in a third refresh operation performed subsequent to the second refresh operation.

12. A method for recycling charge comprising:

momentarily closing one or more switches to transfer charge from one or more power lines of a first array of bit line sense amplifiers involved in a first refresh operation to one or more power lines of at least second and third arrays of bit line sense amplifiers involved in subsequent refresh operations.

13. A circuit configuration for multiple recycling of bit line charges comprising:

one or more common recycle lines;

a plurality of switches, each to selectively couple one or more power lines of a plurality of bit line sense amplifier arrays to the one or more common recycle lines; and

a controller configured to generate a plurality of recycle control signals to control the plurality of switches to sequentially (i) transfer charge from one or more power lines of a first array of bit line sense amplifiers previously involved in a first refresh operation to one or more power lines of a second array of bit line sense amplifiers involved in a second refresh operation performed subsequent to the first refresh operation and (ii) transfer charge from power lines of the first array of bit line sense amplifiers to power lines of a third array of bit line sense amplifiers involved in a third refresh operation performed subsequent to the second refresh operation.

14. The circuit configuration of claim 13, wherein the controller is configured to transfer charge from the one or more power lines of the first array of bit line sense amplifiers to the one or more power lines of the second array of bit line sense amplifiers by:

asserting a first recycle control signal to close a first one or more switches coupling the one or more power lines of the first array of bit line sense amplifiers to the one or more common recycle lines; and

while the first one or more switches is closed, assert a second recycle control signal to momentarily close a second one or more switches coupling the one or more power lines of the second array of bit line sense amplifiers to the one or more common recycle lines.

15. The circuit configuration of claim 14, wherein the controller is configured to transfer charge from the one or more power lines of the first array of bit line sense amplifiers to the one or more power lines of the third array of bit line sense amplifiers and transfer charge from the one or more power lines of the second array of bit line sense amplifiers to the one or more power lines of the third array of bit line sense amplifiers by:

asserting the first recycle control signal to close a first one or more switches coupling the one or more power lines of the first array of bit line sense amplifiers to the one or more common recycle lines;

while the first one or more switches is closed, asserting a third recycle control signal to close a third one or more switches coupling the one or more power lines of the third array of bit line sense amplifiers to the one or more common recycle lines;

de-assert the first recycle control signal to open the first one or more switches; and

while the third one or more switches is closed, asserting the second recycle control signal to momentarily close a second one or more switches coupling the one or more power lines of the second array of bit line sense amplifiers to the one or more common recycle lines.

16. The circuit configuration of claim 14, wherein the controller is further configured to transfer charge from one or more power lines of the first array of bit line sense amplifiers to one or more power lines of at least a fourth array of bit line sense amplifiers involved in at least a fourth refresh operation performed subsequent to the third refresh operation.

17. A memory device comprising:

a plurality of memory cell arrays, each having at least one corresponding array bit line sense amplifiers;

coupling means for selectively coupling one or more power lines of the arrays of bit line sense amplifiers; and

recycle control circuitry configured to, via the coupling means, (i) transfer charge from power lines of a first array of bit line sense amplifiers previously involved in a first refresh operation to power lines of a second array of bit line sense amplifiers involved in a second refresh operation performed subsequent to the first refresh operation and (ii) transfer charge from power lines of the first array of bit line sense amplifiers to power lines of at least a third array of bit line sense amplifiers

involved in at least a third refresh operation performed subsequent to the second refresh operation.

18. The memory device of claim 17, wherein the means for selectively coupling one or more power lines of the arrays of bit line sense amplifiers comprises:

one or more common recycle lines; and

a plurality of sets of one or more switches, each set to couple a corresponding one or more power lines of an associated array of bit line sense amplifiers to the one or more common recycle lines.

19. The memory device of claim 17, wherein the recycle control circuitry is configured to transfer charge from the one or more power lines of the first array of bit line sense amplifiers to the one or more power lines of the second array of bit line sense amplifiers by momentarily closing a first set of one or more switches coupling the one or more power lines of the first array of bit line sense amplifiers to the one or more common recycle lines and while the first set of one or more switches is closed, momentarily closing a second one or more switches coupling the one or more power lines of the second array of bit line sense amplifiers to the one or more common recycle lines

20. The memory device of claim 17, wherein the recycle control circuitry is further configured to, via the coupling means, transfer charge from power lines of the first array of bit line sense amplifiers to power lines of at least a fourth array of bit line sense amplifiers involved in at least a fourth refresh operation performed subsequent to the third refresh operation.

21. The memory device of claim 17, wherein the recycle control circuitry is further configured to, via the coupling means, transfer charge from power lines of the second and third arrays of bit line sense amplifiers to power lines of at least a fourth array of bit line sense amplifiers involved in at least a fourth refresh operation performed subsequent to the third refresh operation.

22. The memory device of claim 17, wherein at least one intermediate refresh operation is performed between the first and second refresh operations, wherein the recycle control circuitry is configured to not transfer charge from power lines of the first array of bit line sense amplifiers to power lines of an array of bit line sense amplifiers involved in the intermediate refresh operation.

23. The memory device of claim 22, wherein after the third refresh operation, the voltage difference between the power lines of the first array of bit line sense amplifiers and a precharge level is approximately 25% of the voltage difference between the precharge level and the voltage level of the power lines immediately after the first refresh operation.